Tutorial 4 - SS2021
Communication Systems and Protocols

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Task 1: Serial Interface

In the figure 1.1 the pulse diagram of a RS232 interface is given. Different transmission frames have been used for the communication. A transmission frame is composed of a start bit ('0'), 5-8 data bits, no (N, none) or one bit for even (E, even) or odd (O, odd) parity, as well as at least 1 or 2 stop bits (‚1'). Possible frame formats are [5..8][N,O,E][1,2], for example 8N1 for 8 data bits, no parity bit and at least 1 stop bit.

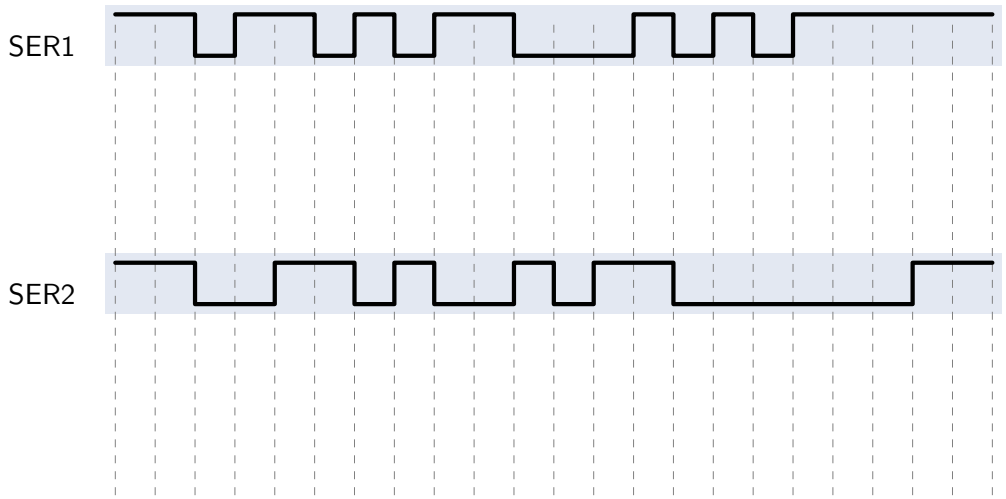

Figure 1.1: Serial interface pulse diagram

A) Give all possible frame formats for the pulse sequences as shown in figure 1.1. All given pulse sequences are describing a correct transmission. Start of a transmission is always the startbit in the third timestep.

B) In the figure below different pulse sequences for a RS232 interface are given. Derive from the figure and the given frame formats if the transmission was error free. Mark the erroneous parts in the pulse diagrams.

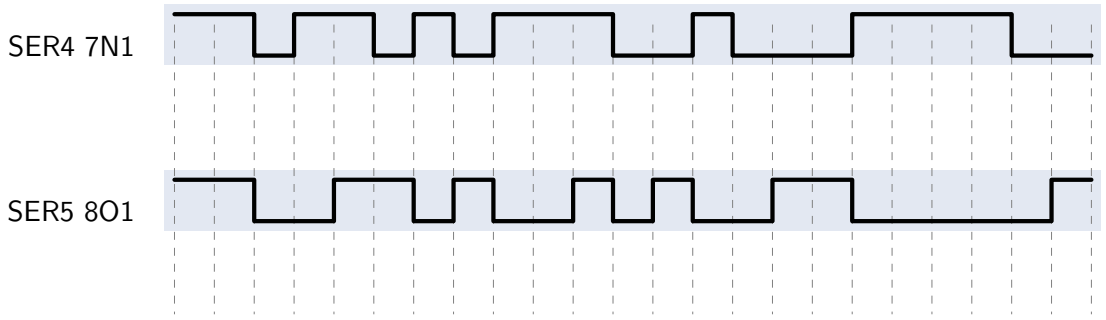

Figure 1.2: RS232 pulse sequences

C) Is it possible to detect errors without knowing the frame formats?

Task 2: Flow-Control

A communication system is given in Figure 2.1. The sender's clock frequency is 1 MHz, the receiver's is 200 kHz. Both partners work synchronously to their own clock signal and try their best to communicate as fast as possible. They apply a Level-triggered Closed-loop Flow Control corresponding to Figure 3.1 for the high-level synchronization.

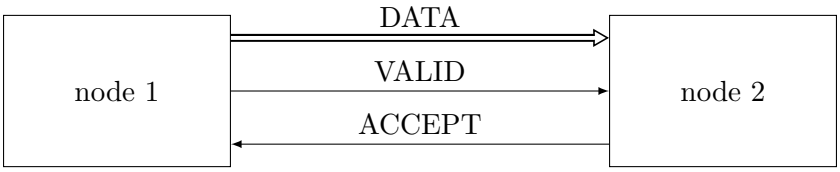

Figure 2.1: Level-triggered Closed-loop Flow Control

A) In Figure 2.2 the sensitive clock edges of the sender and the receiver as well as the signal values for the first sender clock period are shown. In order to avoid violations of setup and hold times, the data is put onto the bus and one clock cycle later the valid signal is set to '1' by the sender. The receiver will also set the accept signal one clock cycle after having received the data. Fill in the progression of all signal lines until the end of the time scale.

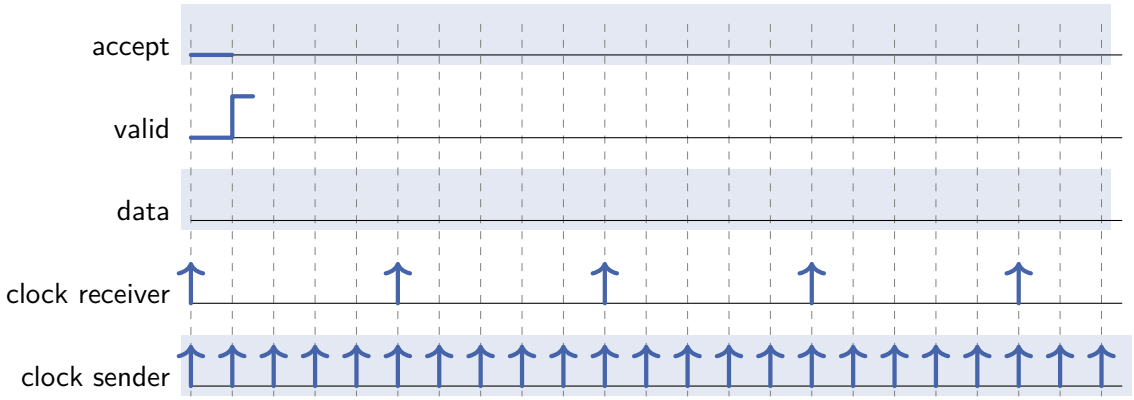

Figure 2.2: Signal progression diagram

B) Is this kind of synchronization free from error in this specific case? Justify your answer.

C) Propose a better solution for this communication scenario.

Task 3: Cyclic Redundancy Check

Task 3.1: Transmission

To protect a data transmission, CRC with the generator polynomial $g(x) = x^2 + 1$ is used.

A) Determine the bit string that is associated with the generator polynomial.

B) What is the length of the checksum that is to be appended to the data stream?

C) Calculate the data stream that will be transmitted if the following bit string is to be protected: 1001010101.

Task 3.2: Reception

In a transmission system that uses CRC for error protection, a sender transmits the following bit stream: 100101010110. Due to interferences during transmission the last 4 bits of the bit stream are flipped before reaching the receiving node.

A) Denote the bit stream as it arrives at the receiving node.

B) Carry out the CRC error detection scheme of the receiver assuming that the generator polynomial $g(x) = x2 + 1$ has been used.
What does the receiver conclude from the result? Explain and discuss the reasons for the receiver's conclusion.

Task 3.3: Hardware implementation

A) To protect data transmissions in a mobile device, the CRC scheme is to be implemented using linear feedback registers with XOR operations. Draw the simplified hardware layout for the polynomial CRC-12 ($x^{12} + x^{11} + x^3 + x^2 + x + 1$).